FIG. 1

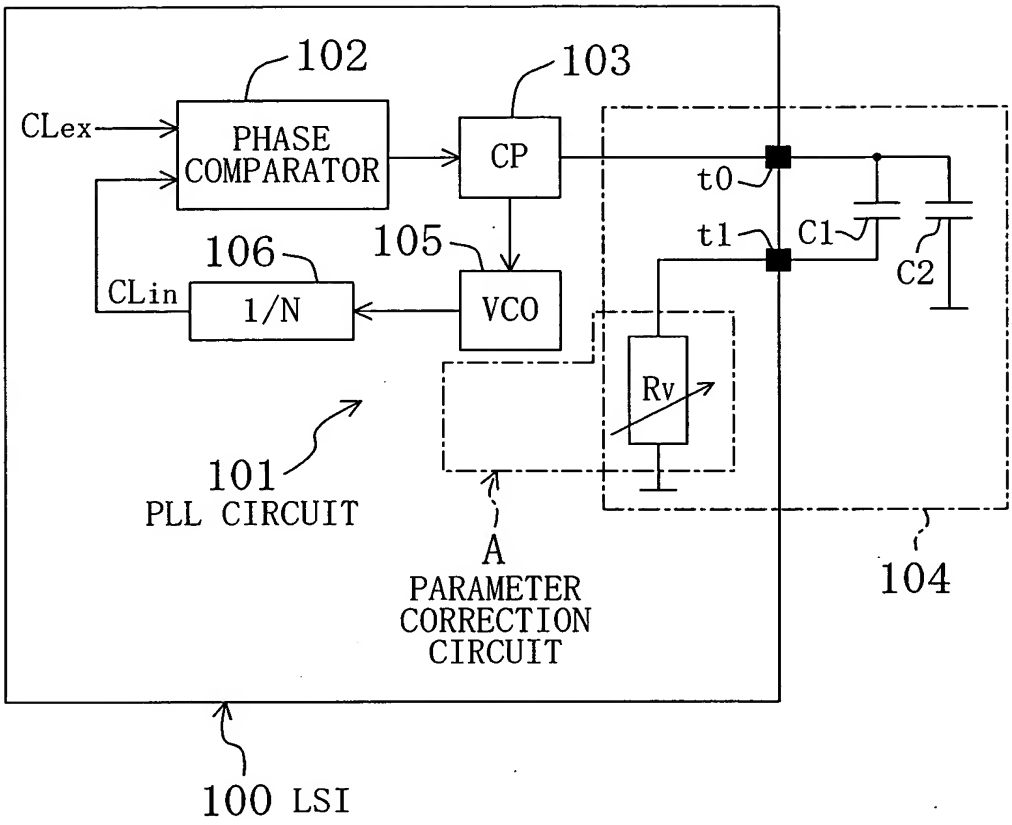

102
103
CLex
PHASE COMPARATOR
CP
t0
t1
C1
C2
106
105
CLin
1/N
VCO
Rv
101
PLL CIRCUIT
A
PARAMETER CORRECTION CIRCUIT
104
100 LSI

FIG. 2A

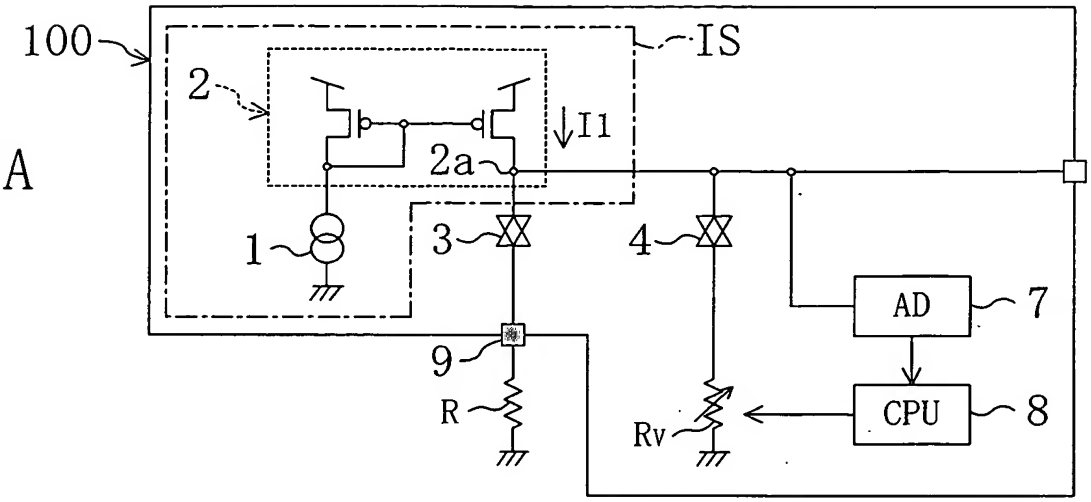


FIG. 2B

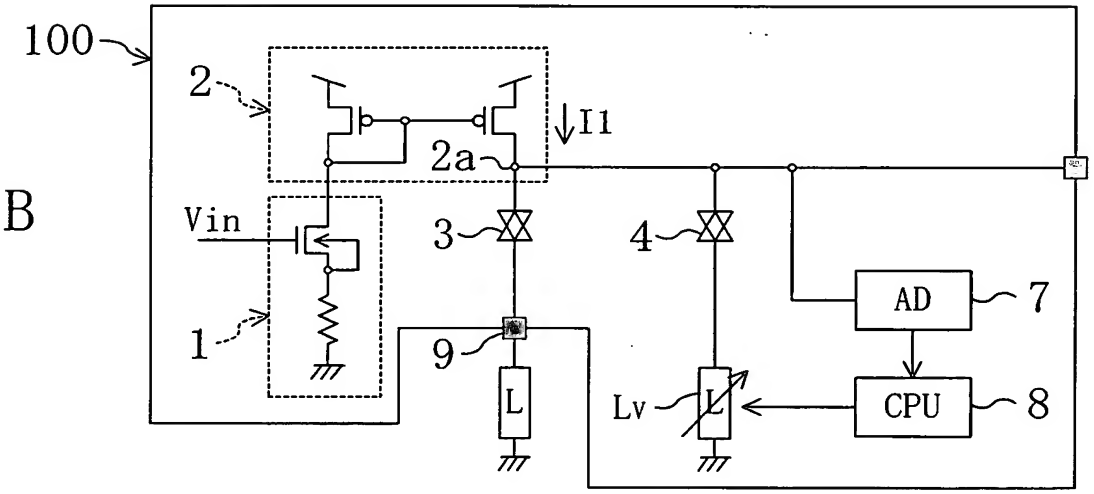


FIG. 2C

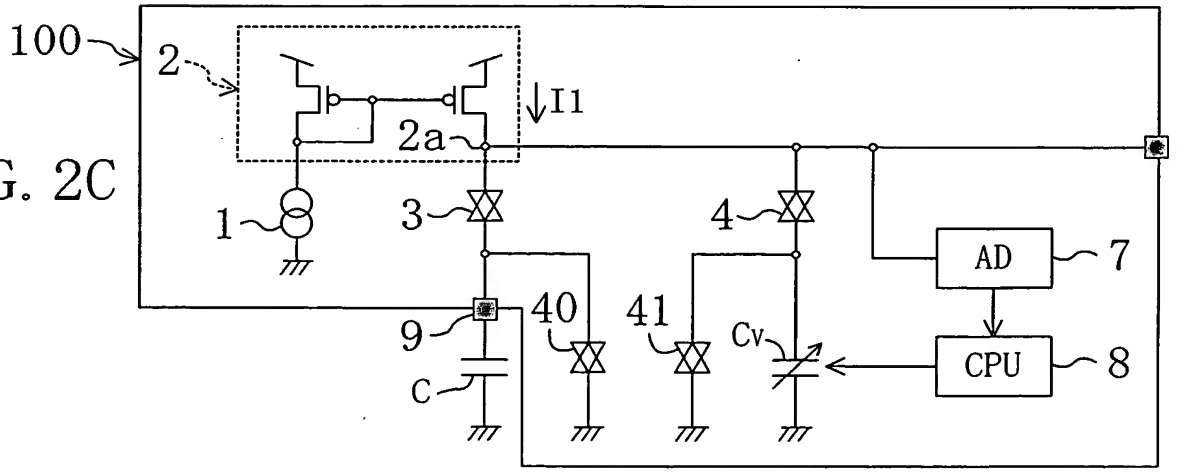


FIG. 3

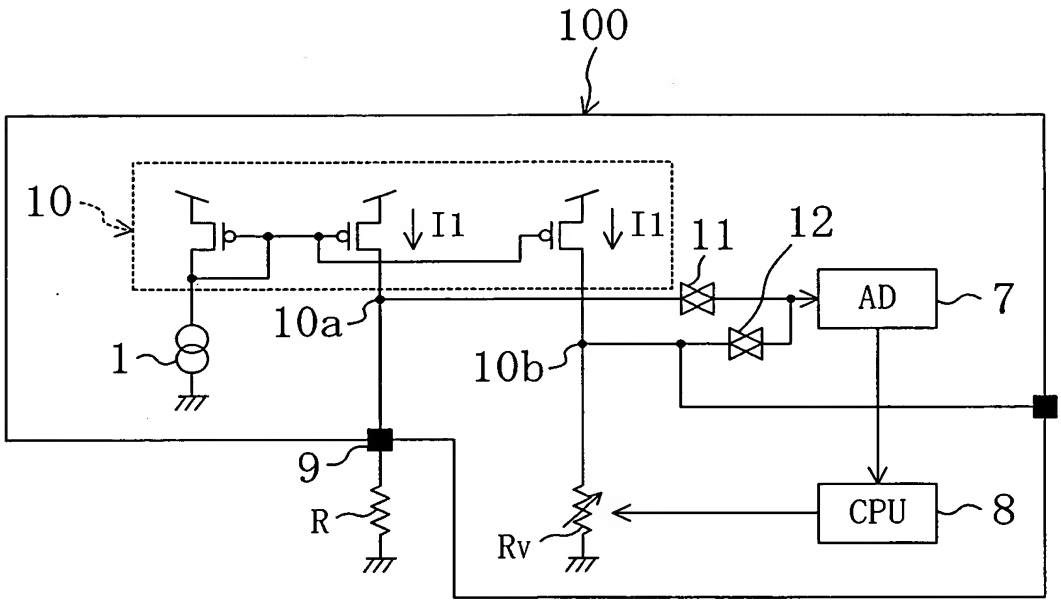


FIG. 4A

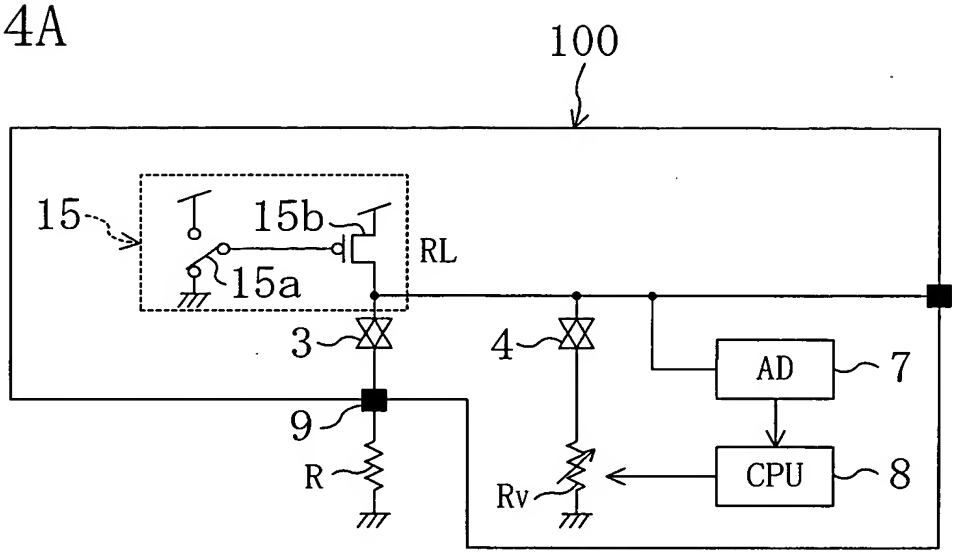

100
15
15b
15a
RL
3
4
AD
7
9
R
Rv
CPU
8

FIG. 4B

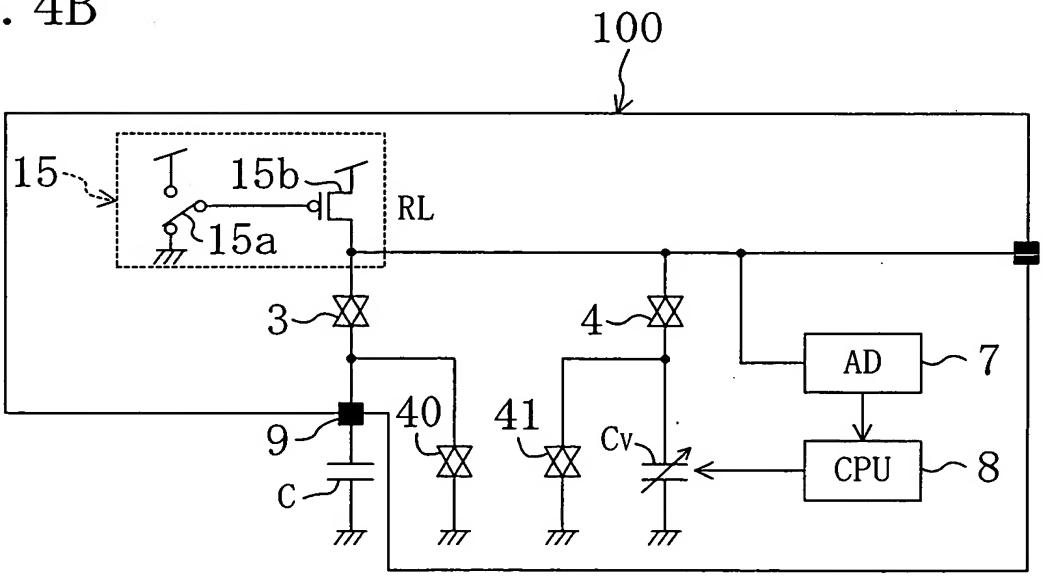

100
15
15b
15a
RL
3
4
AD
7
9
40
41
Cv
C
CPU
8

FIG. 5

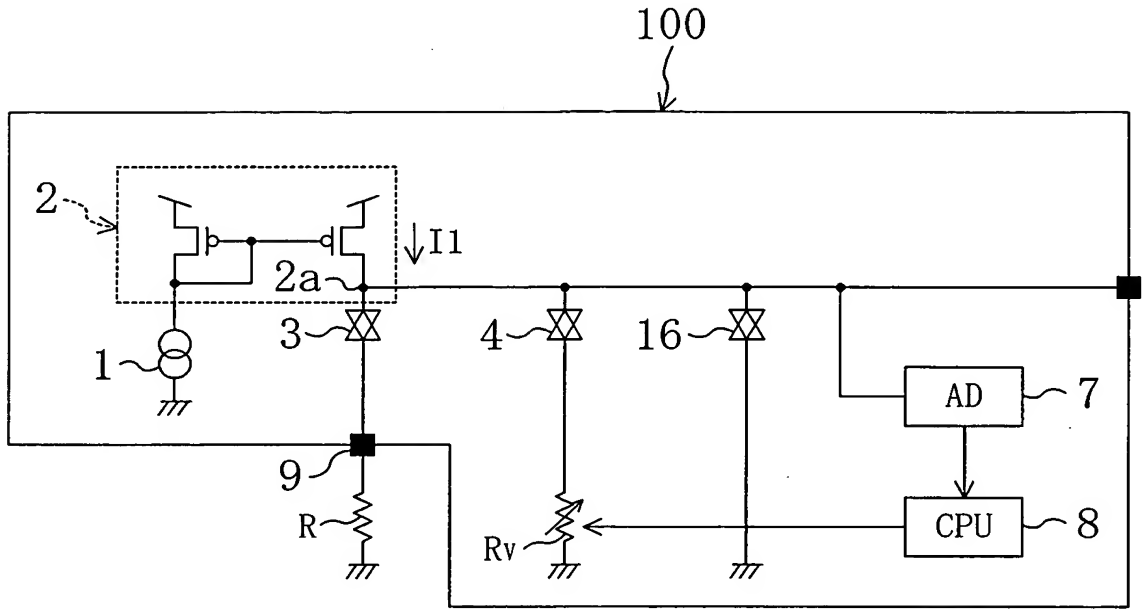

100
2
I1
2a
3
4
16
1
AD
7
9
R
Rv
CPU
8

FIG. 6

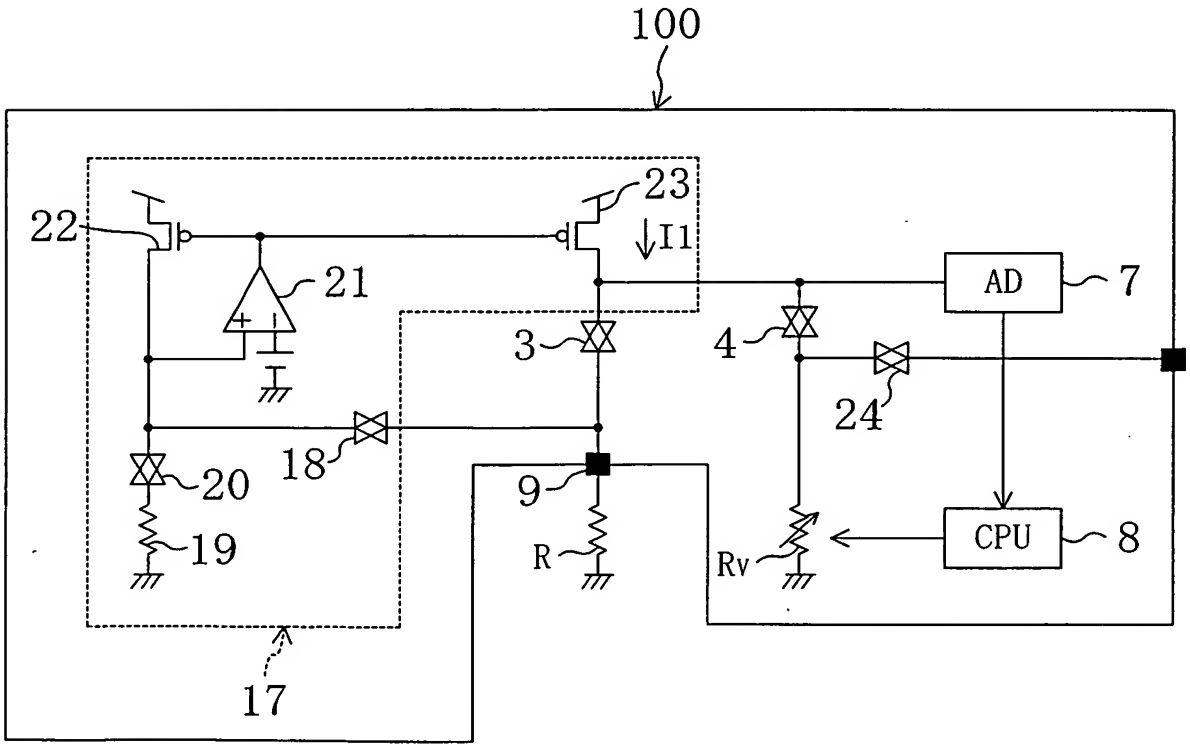

100
22
23
I1
21
AD
7
3
4
24
18
20
9
19
R
Rv
CPU
8
17

FIG. 7A

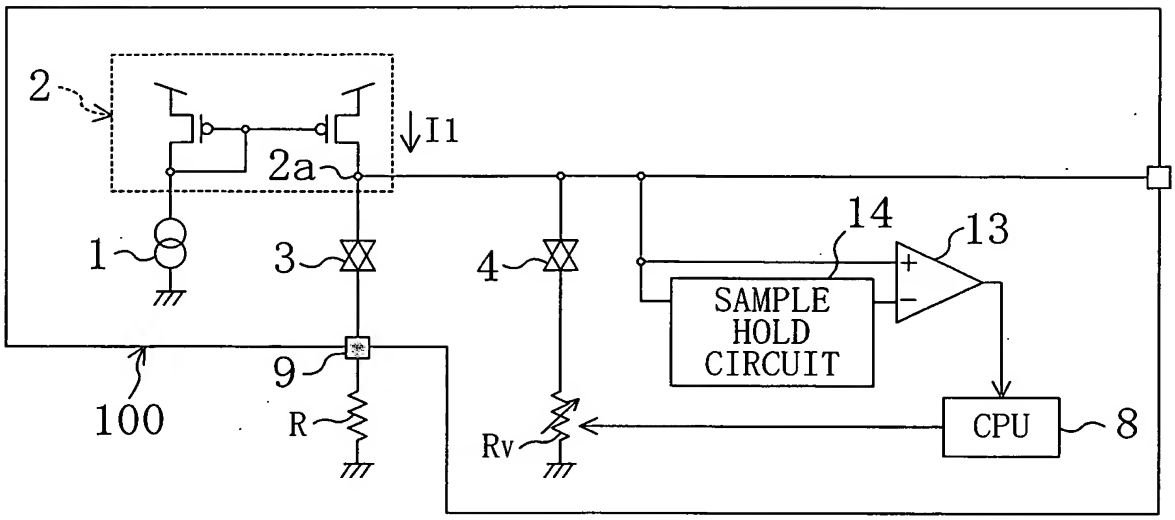


FIG. 7B

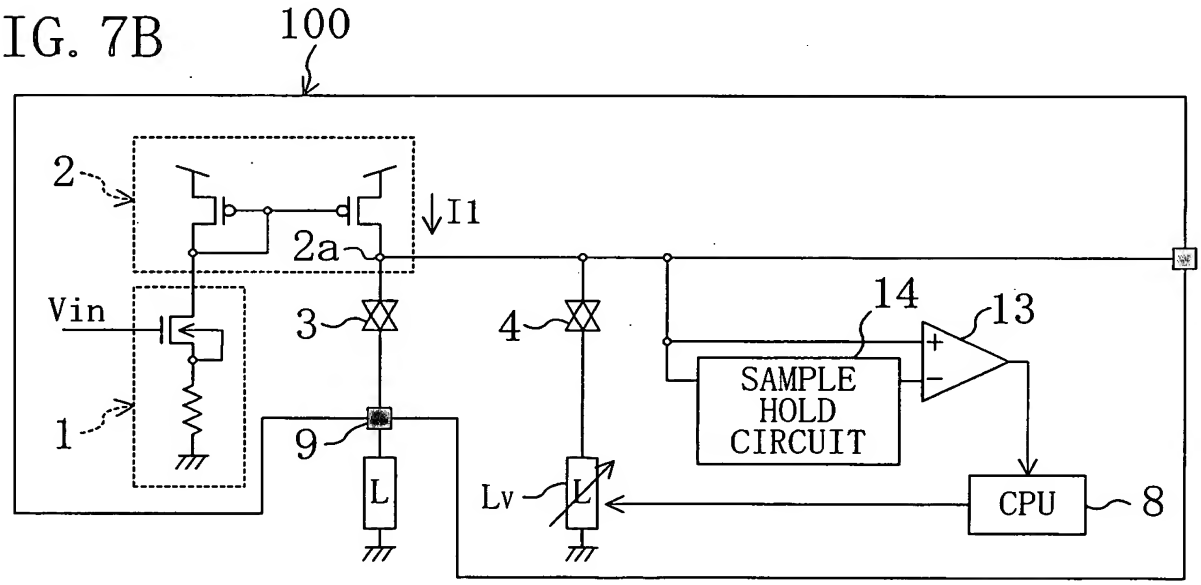


FIG. 7C

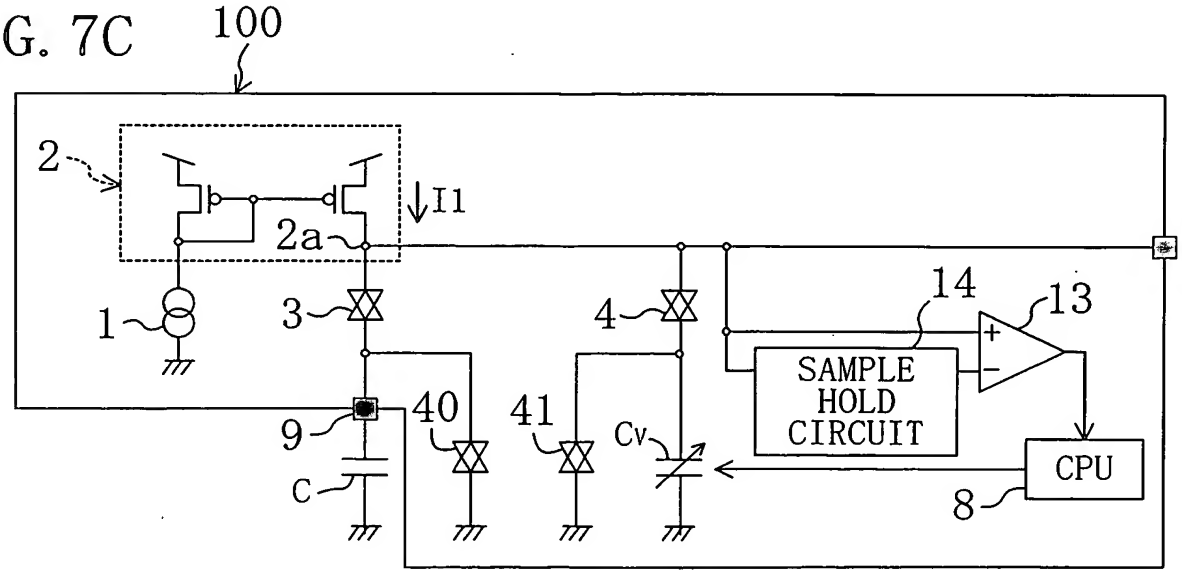


FIG. 8

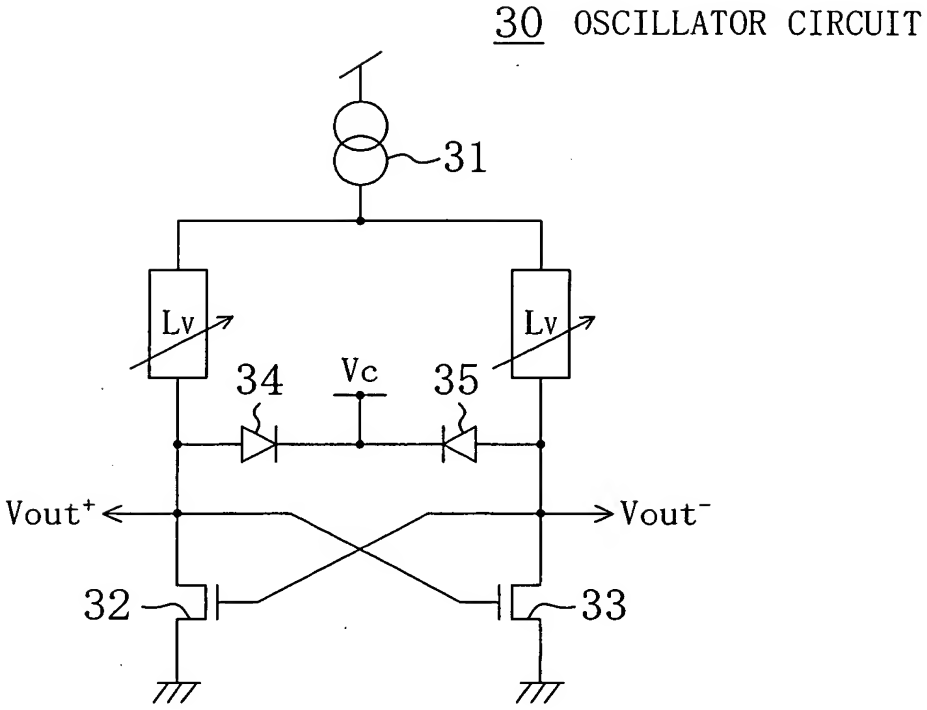


FIG. 9A

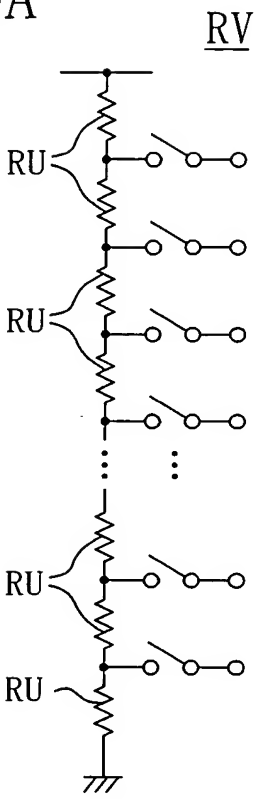


FIG. 9B

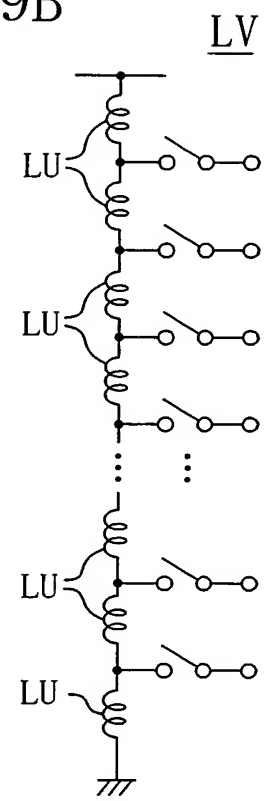


FIG. 9C

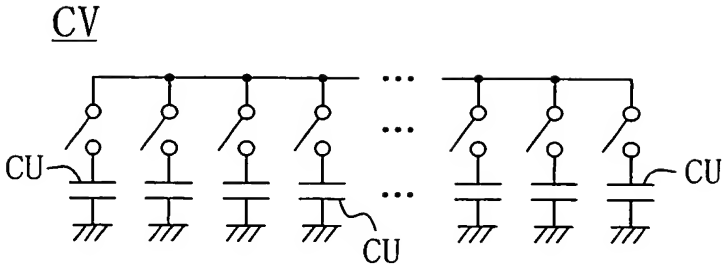


FIG. 10

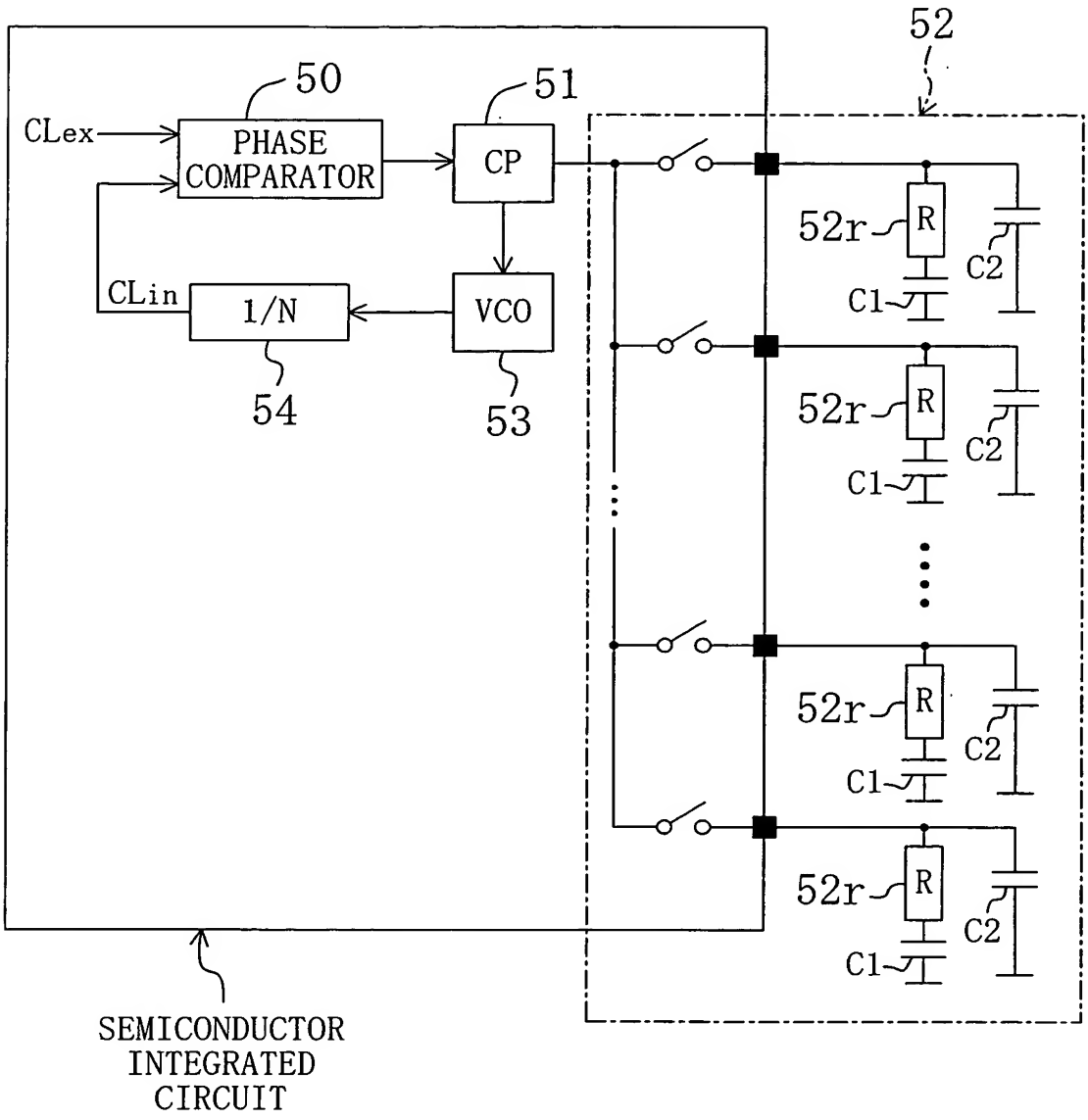

52
50
51
CLex
PHASE COMPARATOR
CP
CLin
1/N
VCO
54
53
52r
R
C1
C2
SEMICONDUCTOR INTEGRATED CIRCUIT

FIG. 11

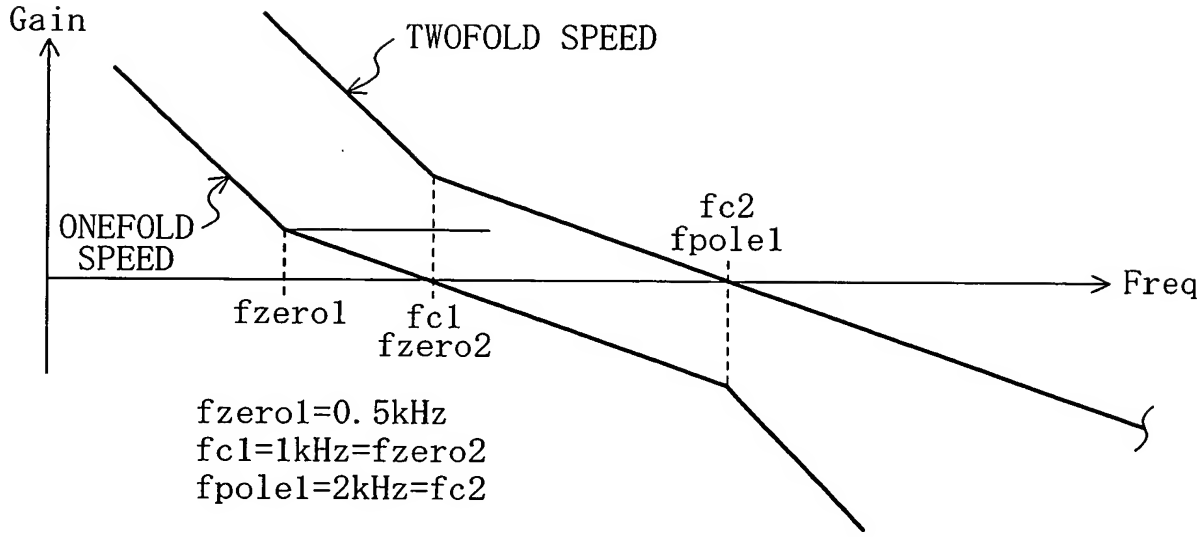
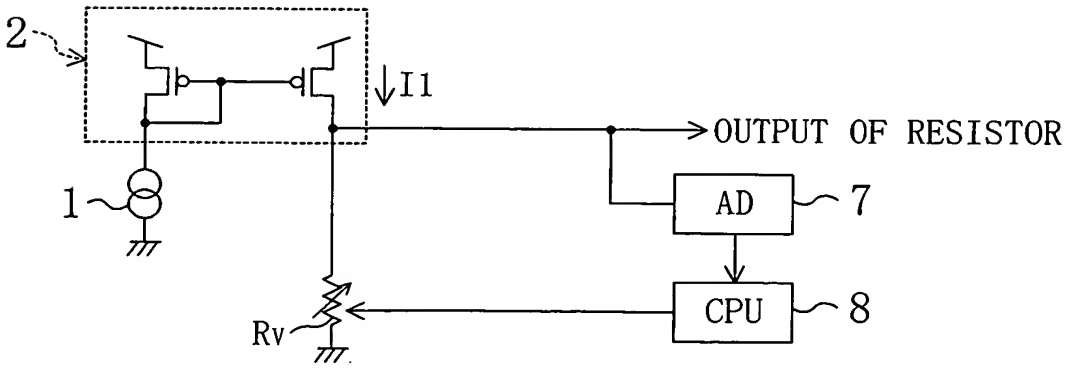

Gain
TWOFOLD SPEED
ONEFOLD SPEED
fc2
fpole1
Freq
fzero1
fc1
fzero2
fzero1=0.5kHz
fc1=1kHz=fzero2
fpole1=2kHz=fc2

FIG. 12


2
I1
OUTPUT OF RESISTOR
1
AD
7
CPU
8
Rv